We Claim:

1. A method for testing configurable logic blocks in an emulation system, the method comprising steps of:

configuring a first set of configurable logic blocks to be first testing circuitry; and

operating the first set to test a second set of configurable logic blocks.

2. The method of claim 1, further comprising steps of:

configuring the second set to be second testing circuitry; and

operating the second set to test the first set.

3. The method of claim 1, further comprising steps of:

configuring a third set of configurable logic blocks to be second testing circuitry; and

operating the third set, concurrently with the first set, to test a fourth set of configurable logic blocks.

4. The method of claim 3, further comprising steps of:

configuring the second set and the fourth set to be third testing circuitry and fourth testing circuitry, respectively; and

operating the second set and the fourth set to test the first set and the third set, respectively.

5. The method of claim 1, wherein the step of configuring the first set includes:

configuring $N \geq 1$ configurable logic blocks of the first set to operate as an N-bit input generator; and

coupling an output of the N-bit input generator to the configurable logic blocks of the second set.

6. The method of claim 5, further comprising a step of configuring a configurable logic block of the first set to determine whether the N-bit input generator outputs a predetermined value.

7. The method of claim 5, wherein the step of configuring the $N \geq 1$ configurable logic blocks includes configuring the $N \geq 1$ configurable logic blocks to operate as an N-bit counter.

8. The method of claim 7, wherein the predetermined value is a maximum value of the N-bit counter.

9. The method of claim 1, further comprising a step of configuring each configurable logic block of the second set to respond with a deterministic output to an N-bit input,

wherein the step of configuring the first set includes configuring a configurable logic block of the first set as a verifier to verify a responsive output of the second set organized into M groups of configurable logic blocks.

10. The method of claim 9, wherein the verifier is configured to accept the N-bit input, and wherein each of the M groups includes N–1 configurable logic blocks configured to supply N–1 bits to the verifier.

11. The method of claim 9, wherein the verifier is configured to accept its own output as one bit of the N-bit input.

12. The method of claim 11, wherein the step of configuring the verifier includes configuring the verifier to deterministically output a failure indicator.

13. A method of testing routing portions in an emulation system, the method comprising steps of:

configuring a first routing portion to map N inputs of the first routing portion to N outputs of the first routing portion in a first configuration;

configuring a second routing portion to map N inputs of the second routing portion to N outputs of the second routing portion in a second configuration inverse to the first configuration, the N inputs of the second routing portion configured to be coupled to the N outputs of the first routing portion;

applying input data to the inputs of the first routing portion; and

receiving output data from the output of the second routing portion, the output data being responsive to the input data.

14. The method of claim 13, further comprising a step of determining whether a difference exists between the input data and the output data.

15. The method of claim 13, further comprising a step of configuring a first group of configurable logic blocks to perform the step of applying, wherein the configurable logic blocks include logic circuitry for implementing reprogrammable logic.

16. The method of claim 15, further comprising a step of configuring a second group of configurable logic blocks to perform the step of determining.

17. The method of claim 13, wherein the N inputs of the second routing portion are configured to be coupled to the N outputs of the first routing portion through at least one reconfigurable interconnect.

18. An integrated circuit, comprising:

a first set of configurable logic blocks;

a second set of configurable logic blocks, coupled to the first set; and

a data processing portion coupled to the first set, the data processing portion configured to provide a first test pattern to the first set,

wherein the first set is configured to provide a second test pattern to test the second set, and the second set is configured to output data in response to the second test pattern received from the first set.

19. The integrated circuit of claim 18, wherein the first set is further configured to compare the output data to predetermined output data.

20. The integrated circuit of claim 18, wherein the data processing portion is further configured to provide a third test pattern to the second set, the second set is further configured to provide a fourth test pattern to test the first set, and the first set is further configured to output second data in response to fourth test pattern received from the second set.

21. The integrated circuit of claim 18, wherein the first set is further configured to provide an *N*-bit input generator to the second set and to provide a configurable logic block as a verifier to verify the output data of the second set.

22. The integrated circuit of claim 21, wherein an output of the verifier is an input to the verifier, and wherein the output of the verifier is a failure indicator.

23. An integrated circuit, comprising:

a first routing portion configured to map *N* inputs of the first routing portion to *N* outputs of the first routing portion in a first configuration, and configured to receive input data;

a second routing portion configured to map *N* inputs of the second routing portion to *N* outputs of the second routing portion in a second configuration inverse to the first configuration, and configured to output data; and

monitoring logic configured to determining whether a difference exists between the input data and the output data,

wherein the *N* inputs of the second routing portion are coupled to the *N* outputs of the first routing portion.

24. An emulation system, comprising:

a plurality of emulation boards; and

a plurality of interconnect boards interconnecting the plurality of emulation boards,

wherein each of the plurality of interconnect boards has an integrated circuit having first and second sets of configurable logic blocks and a data processing portion coupled to the first and second sets, wherein the data processing portion is configured to provide a first test pattern to the first set to test the second set and a second test pattern to the second set to test the first set.

25. An emulation system, comprising:

a plurality of emulation boards; and

a plurality of interconnect boards interconnecting the plurality of emulation boards,

wherein each of the plurality of interconnect boards has an integrated circuit having first and second routing portions and monitoring logic,

wherein the first routing portion is configured receive input data and to map *N* inputs of the first routing portion to *N* outputs of the first routing portion in a first manner,

wherein the second routing portion is configured to map *N* inputs of the second routing portion to *N* outputs of the second routing portion in a second manner inverse to the first manner, and is configured to output data, and

wherein the monitoring logic is configured to determining whether a difference exists between the input data and the output data.